REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

Claims 1-12, 14-18, and 20 are pending in this application. Claim 13 is canceled by the present response without prejudice, claim 19 having previously been canceled without prejudice. Claim 13 was objected to under 37 C.F.R. § 1.75(c). Claims 1-20 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. patent 4,663,644 to Shimizu.

Addressing first the objection to claim 13, that objection is obviated by the present response as claim 13 is canceled by the present response.

Addressing now the rejection of claims 1-20 under 35 U.S.C. § 102(b) as anticipated by Shimizu, that rejection is traversed by the present response.

Initially, applicants note each of the independent claims is amended by the present response to clarify a feature recited therein. Specifically, independent claim 1 now clarifies the first gate insulating film formed "on both of sidewall-surfaces opposed to each other" of the first gate electrode group; the other independent claims now also recite similar features. No new matter is believed to be added by that amendment.

With such a claimed structure, as the first insulating film is not formed only on the main sidewall surface, but is also formed on the other sidewall surface opposite to the main sidewall surface, a channel region can be formed on both of sidewall surface regions in a semiconductor device. As shown in Figure 8 in the present specification as a non-limiting example, channel regions 25 can be formed on both of sidewall-surface regions. As a result, an area of a channel region in the semiconductor device of the claimed invention can be significantly increased. Further, since a greater number of channel regions can be formed in a given area with a minimum design space, a channel density can be increased, and the device resistance for a MOSFET can be lowered.

Applicants respectfully submit Shimizu does not disclose or suggest such a structure.

The outstanding Office Action relies upon the gate insulating film 2 in Shimizu to meet the limitations of the claimed "first gate insulating film". However, in that respect applicants note film 2 is only formed on a first main sidewall surface and a bottom surface of the gate electrode of a pair of the MOSFETs in Shimizu. That is, that insulating film 2 is not formed on both of sidewall surfaces that are opposed to each other of a gate electrode. As shown for example in the figures in Shimizu a different film 5 opposes the film 2. In Shimizu the insulating film 2 acting on the gate is ***only*** formed on the main sidewall surface and a bottom surface.

Moreover, with such a structure the device of Shimizu cannot achieve one of the realized benefits of the present invention of forming a channel region on both of sidewall surface regions in a semiconductor device.

In view of these foregoing comments, applicants respectfully submit the claims as currently written distinguish over Shimizu.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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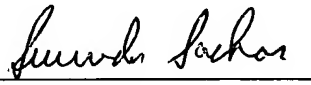
MAIER & NEUSTADT, P.C.



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